Amendments To the Claims

Claim 1 (Currently amended): A power chip resistor comprising:

a first and second film resistor each having (a) a substrate with a top surface, a bottom surface, a first end surface, an opposing end surface, a first side surface and an opposing side surface, (b) a film resistive element on the top surface of each substrate, (c) an end cap on the first end surface and electrically connected to the film resistive element, (d) a second end cap on the opposing end surface and electrically connected to the film resistive element, and (e) each end cap extending onto the top surface, the bottom surface, the first side surface and the second side surface;

the second film resistor of approximately the same physical size as the first film resistor, the second film resistor of approximately the same orientation as the first film resistor;

an encapsulant of glass frit between the top surface of the first film resistor and the bottom surface of the second film resistor;

a first nickel barrier plating electrically connecting the end cap on the first end surface of the substrate of the first film resistor and the first end surface of the substrate of the second film resistor and mechanically bonding the film resistors without adhesive;

a second nickel barrier plating electrically connecting the second end cap on the second end surface of the substrate of the first film resistor and the second end cap on the second end surface of the substrate of the second film resistor and mechanically bonding the film resistors without adhesive;

whereby the first and second nickel barrier plating used to connect the end caps and the encapsulant provide long-term mechanical stability and resistance to resistive heating~~.~~;

wherein the power chip resistor is flow solderable due to the resistance to resistive heating provided by the first and second nickel barrier plating.

Claim 2 (Previously presented): The power chip resistor of claim 2 wherein the film resistive elements are thick film resistive elements.

Claim 3 (Previously presented): The power chip resistor of claim 1 wherein the film resistive elements comprise ruthenium oxide.

Claims 4-8 (Canceled).

Claim 9 (Currently amended): A power chip resistor comprising:

a first and second film resistor each having (a) a substrate with a top surface, a bottom surface, a first end surface, an opposing end surface, a first side surface and an opposing side surface, (b) a film resistive element on the top surface of each substrate, (c) an end cap on the first end surface of each surface electrically connected to the film resistive element, and (d) a second end cap on the opposing end surface of each substrate and electrically connected to the film resistive element; a glass frit encapsulant between the top surface of the substrate of the first film resistor and the bottom surface of the substrate of the second film resistor;

a first metal barrier plating covering and being electrically connected to the end caps on the first end surface of the substrate of the first and second film resistors and mechanically bonding the film resistors without adhesive;

a second metal barrier plating covering and being electrically connected to the second end caps on the opposing end surface of the substrate of the first and second film resistors and mechanically bonding the film resistors without adhesive to provide long term mechanical stability and resistance to resistive heating~~,~~;

wherein the power chip resistor is flow solderable due to the resistance to resistive heating provided by the first and second nickel barrier plating.

Claim 10 (Previously presented): The power chip resistor of 9 wherein the first and second metal barriers comprise a nickel alloy.

Claim 11 (Previously presented): The power chip resistor of 10 wherein the first and second metal barriers comprise nickel.

Claim 12 (Previously presented): The power chip resistor of claim 9 wherein the film resistive elements comprise ruthenium oxide.

Claims 13-15 (Canceled).

Claim 16 (Previously presented): The power chip resistor of claim 9 further comprising:

a third film resistor having (a) a substrate with a top surface, a bottom surface, a first end surface, an opposing end surface, a first side surface and an opposing side surface, (b) a film resistive element on the top surface of the substrate, (c) an end cap on the first end surface electrically connected to the film resistive element, and (d) a second end cap on the opposing end surface and electrically connected to the film resistive element;

a second encapsulant of glass frit between the top surface of the substrate of the second film resistor and the bottom surface of the substrate of the third film resistor, the first nickel barrier electrically connected to the end cap of the first end surface of the third film resistor, the second nickel barrier electrically connected to the second end cap on the second end surface of the third film resistor.

Claim 17 (Previously presented): The power chip resistor of claim 16 further comprising:

a fourth film resistor having (a) a substrate with a top surface, a bottom surface, a first end surface, an opposing end surface, a first side surface and an opposing side surface, (b) a film resistive element on the top surface of the substrate, (c) an end cap on the first end surface electrically connected to the film resistive element, and (d) a second end cap on the opposing end surface and electrically connected to the film resistive element; a third encapsulant of glass frit between the top surface of the substrate of the third film resistor and the bottom surface of the substrate of the fourth film resistor, the first nickel barrier electrically connected to the end cap of the first end surface of the fourth film resistor, the second nickel barrier electrically connected to the second end cap on the second end surface of the fourth film resistor.

Claim 18 (Currently amended): A stacked chip resistor comprising:

a first chip resistor and a second chip resistor, each chip resistor having a substrate with a thick film resistive element attached to the substrate, a first end cap and a second end cap, each end cap being an electrical terminal connected to the thick film resistive element and fully covering a first or second end surface of the substrate;

a layer of glass frit placed between the first chip resistor and the second chip resistor;

a first nickel barrier plating, the nickel barrier plating electrically connecting and surrounding the first end cap of the first chip resistor and the first end cap of the second chip resistor;

a second nickel barrier plating, the nickel barrier plating electrically connecting and surrounding the second end cap of the first chip resistor and the second end cap of the second chip resistor;

the nickel barriers bonding the chip resistors without adhesive and thereby providing long-term mechanical stability and resistance to resistive heating~~.~~;

wherein the power chip resistor is flow solderable due to the resistance to resistive heating provided by the first and second nickel barrier plating.

Claim 19 (Canceled).

Claim 20 (Original): The stacked chip resistor of claim 18 wherein the first film resistor and the second film resistor further have ruthenium oxide resistive elements.

Claim 21 (Canceled).

Claim 22 (Original): The stacked chip resistor of claim 18 wherein each end cap is a silver alloy.

Claim 23 (Original): The stacked chip resistor of claim 22 wherein each end cap is a silver palladium.

Claim 24 (Previously presented): The stacked chip resistor of claim 18 further comprising:

a third chip resistor, the third chip resistor having a substrate with a thick film resistive element attached to the substrate, a first end cap and a second end cap, each end cap being an electrical terminal connected to the thick film resistive element,;

a second layer of glass frit placed between the second chip resistor and the third chip resistor, the first nickel barrier electrically connected to the first end cap of the third chip resistor, the second nickel barrier electrically connected to the second end cap of the third chip resistor.

Claim 25 (Previously presented): The stacked chip resistor of claim 24 further comprising:

a fourth chip resistor, the fourth chip resistor having a substrate with a thick film resistive element attached to the substrate, a first end cap and a second end cap, each end cap being an electrical terminal connected to the thick film resistive element, the second chip resistor, and the third chip resistor;

a third layer of glass frit placed between the third chip resistor and the fourth chip resistor, the first nickel barrier electrically connecting the first end cap of the fourth chip resistor with the first end cap of the first chip resistor and the first end cap of the second chip resistor and the first end cap of the third chip resistor, the second nickel barrier electrically connected to the second end cap of the fourth chip resistor.

Claims 26-29 (Canceled).

Claim 30 (Currently amended): A power chip resistor comprising:

a first and second film resistor each having (a) a substrate with a top surface, a bottom surface, a first end surface, an opposing end surface, a first side surface and an opposing side surface, (b) a film resistive element on the top surface of each substrate, (c) an end cap on the first end surface covering substantially all of the first end surface, and electrically connected to the film resistive element, (d) a second end cap on the opposing end surface covering substantially all of the opposing end surface and electrically connected to the

film resistive element, and (e) each end cap extending on to the top surface, the bottom surface, the first side surface and the second side surface;

the second film resistor of approximately the same physical size as the first film resistor, the second film resistor of approximately the same orientation as the first film resistor;

an encapsulant between the top surface of the first film resistor and the bottom surface of the second film resistor;

the encapsulant separating the top surface of the first film resistor and the bottom surface of the second film resistor such that the top surface of the first film resistor is not in contact with the bottom surface of the second film resistor;

a first barrier electrically connecting the end cap on the first end surface of the first film resistor and the first end surface of the second film resistor and mechanically bonding the film resistors without adhesive;

a second barrier electrically connecting the second end cap on the second end surface of the first film resistor and the second end cap on the second end surface of the second film resistor and mechanically bonding the film resistors;

the first barrier extending from the portion of the first end cap on the top surface of the first film resistor to the portion of the first end cap on the bottom surface of the second film resistor;

the second barrier extending from the portion of the second end cap on the top surface of the first film resistor to the portion of the second end cap on the bottom surface of the second film resistor;

whereby the first and second barrier provide long-term mechanical stability and resistance to resistive heating.

Claim 31 (Currently amended): A stacked power chip resistor, comprising:

a first chip resistor and a second chip resistor, each chip resistor comprising a substrate, a resistive element on the substrate and first and second end caps electrically connected to opposite ends of the resistive element;

an inert encapsulant between the first chip resistor and the second chip resistor;

a first barrier mechanically connecting the first end cap of the first chip resistor and the first end cap of the second chip resistor to provide long term mechanical stability in a manner resistant to resistive heating;

a second barrier mechanically connecting the second end cap of the first chip resistor and the second end cap of the second chip resistor to provide long term mechanical stability in a manner resistant to resistive heating.